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L16	4	"6308260"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/28 16:56
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S1	17	"5887161"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 15:14

S2	4	"6308260"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 17:03
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S5	10	"5913048"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 14:44
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S7	0	(operand near depedenc\$5) and (rename\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 17:59
S8	115	(operand near dependenc\$5) and (rename\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 17:59
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S10	6	((("5950533") or ("5974524") or ("6035394"))).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 18:16

S11	12	"5974524"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/24 18:16
S12	2	("5887161").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 14:22
S13	15	"5996085"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/28 16:54
S14	2	("5887161" "5913048").pn. and (instruction adj queue)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 15:15
S36	2	("6496855").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 18:42
S37	6	((("6199079") or ("6460042") or ("6249779"))).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/25 18:42
S38	3	("6505046").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/03/28 13:43

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Tip: Try removing quotes from your search to get more results.

United States Patent Application: 0040215936

... instruction at its designated issue **queue** address (IQP ... the CTB bits selects the **rename register** array at ... Valid state, then the **issuing instruction** defaults to ...
appft1.uspto.gov/. .../%22thread - 56k - Supplemental Result - [Cached](#) - [Similar pages](#)

EP1256053

... the ITAG associated with a particular **queue** entry or ... registers must be allocated
a **rename register** in the ... three issue slots from all **issuing instruction** in the ...
swpat.ffii.org/pikta/txt/ep/1256/053/ - 91k - [Cached](#) - [Similar pages](#)

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... 194 9.5 Instruction Dispatch, and the DFM **Queue** 195 9.6 Data Flow ...
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 Results 1 - 10 of about 14 for **"issue instruction" "rename register" "queue"**. (0.21 second)

POWER4 System Microarchitecture -- Page 3

Group Dispatch and Instruction **Issue**: **Instruction** groups are dispatched ... sits in the issue **queue** until data ... **Rename Register**: For each register that is renamed ...

www-1.ibm.com/servers/eserver/pseries/hardware/whitepapers/power4_3.html - 39k - [Cached](#) - [Similar pages](#)

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... Div . FP mult . Int unit Wait **queue** Register file scoreboard issue ... X X X LD F6, 34(R2) Write result Execute **Issue Instruction** Mult1 Mem[34+Reg[R2]] Div Y Mult2 ...

www.cs.pitt.edu/~melhem/courses/2410/ch3_a.pdf - [Similar pages](#)

[PDF] ECE/CS 752 ECE/CS 752 Register Data Flow Register Data Flow ...

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... HOLD DISPATCHING UNTIL RESOLUTION OF DEPENDENCE ALLOW DECODING OF SUBSEQUENT INSTRUCTIONS **RENAME REGISTER** HARDWARE ALLOCATION ... Pending Target Return **Queue** ...

homepages.cae.wisc.edu/~mikko/752/lect8-register-dataflow.pdf - [Similar pages](#)

[PPT] ECE/CS 752: Midterm 1 Review

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... When all operands ready, **issue instruction** into Functional Unit (FU) and deallocate RS entry (no further stalling in ... Issue **Queue**. ... **Rename register** organization. ...

homepages.cae.wisc.edu/~mikko/752/midterm1-review.ppt - [Similar pages](#)

[PDF] IBM ^ POWER4 System Microarchitecture

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... Group Dispatch and Instruction **Issue**: **Instruction** groups are dispatched into the issue queues ... Table 1 summarizes the depth of each issue **queue** and the number ...

www.parallab.uib.no/resources/regatta/documents/power4.pdf - [Similar pages](#)

Decode, Rename & Dispatch Unit

... the pipeline and starts the multiple **issue instruction** level parallelism ... sends the address of that **Rename Register** to the ... is implemented as a FIFO **queue** for the ...

sashisu.tripod.com/projects/ece442/ece442_project_new.htm - 39k - [Cached](#) - [Similar pages](#)

[PDF] "Tomasulo's Algorithm"

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... Lec ture 9 Page 4 Attached **Rename Register** File to ROB Data Busy Tag ARF M ap Table ... Pending Target Return **Queue** FAD 3 2 1 FAD 3 2 1 OP T S1 S2 S3 OP T S1 S2 S3 ...

www.cise.ufl.edu/~peir/cda6159/Lecture-09.pdf - Supplemental Result - [Similar pages](#)

[PDF] Lecture 9 Compiler and Hardware Support for ILP

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... basic stages – Fetch : Loads decode **queue** with up ... and prepares them for **issue** – **Instruction** issue: Issues ... station and allocates **rename register** and reorder ...

www.eecs.lehigh.edu/~mschulte/ece401-99/lect/my-lec09-p6.pdf - [Similar pages](#)

[PDF] Generic Datapath Alternatives of Advanced Superscalar Processors

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... **Instruction** issue policies of superscalar processors ... **rename register** files are used

exclusively for renaming. ... are held in the same ROB **queue** despite using ...
www.lpds.sztaki.hu/highlights/aca/resources/DPATH.pdf - [Similar pages](#)

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... Group dispatch and instruction **issue instruction** groups are dispatched ... sits in the
issue **queue** until the ... **Rename register**: For each register that is renamed ...
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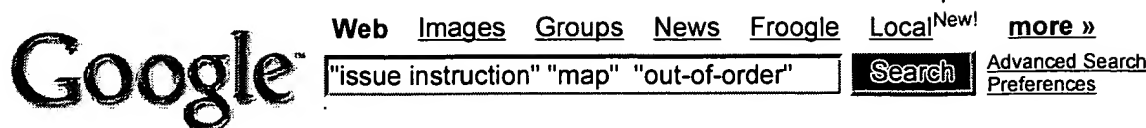
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[PDF] [Superscalar Processors Ch 14 Superscalar Processing New dependency ...](#)

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... if any stalls needed, do them before **issue** • **Instruction** reorder and commit ... get next ISA instruction (rarely) • **map** it to ... Pipeline **Out-of-Order** Execution ...
www.cs.helsinki.fi/u/kerola/tikra/s2002/luennot/ch14_p6.pdf - [Similar pages](#)

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... now with no stalls – if any stalls needed, do them before **issue** • **Instruction** reorder and ... **out-of-order** issue • See the effect of ... **map** it to pops ...
www.cs.helsinki.fi/u/kerola/tikra/s2002/luennot/ch14_p2.pdf - [Similar pages](#)

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... Renames all destination registers: **Out-of-order** write does not ... free (no structural hazard), **issue instruction** & operand ... Dynamically **map** names to locations. ...
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... Renames all destination registers: **Out-of-order** write does not ... If reservation station free (no structural hazard), **issue instruction** & operand ...
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... hazards by stalling instructions. x "Better Solution": **Issue instruction out of order**, Use register ... q **Out of order** execution ... Decode Register **map** table ...
www.cs.duke.edu/~raw/cps104/Lectures/L20SS.pdf - [Similar pages](#)

[PDF] [Predicate Prediction for Efficient Out-of-order Execution](#)

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... to reduce the pressure on the **issue/instruction** queue ... general problem is faced by all **out-of-order** IA64 implementations ... a single tag in the register **map**, and an ...
www.princeton.edu/~echi/other/predicate-prediction-for-efficient.pdf - [Similar pages](#)

[PDF] [Freelance Graphics - wced2002.PRZ](#)

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... What is the Problem? **Out of order** superscalars achieve high **Out of order** superscalars achieve high ... such as predication. Instruction **Issue: Instruction** Issue: ...
www.research.ibm.com/vliw/Pdf/wced02_slides.pdf - [Similar pages](#)

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... the scheduler can not **issue instruction** 2 to ... Essentially, they **map** the x86 registers via a table ... a difference register renaming and **out of order** execution makes ...
www.aceshardware.com/Spades/read.php?article_id=53-53k - [Cached](#) - [Similar pages](#)

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... **order** issue with **out-of-order** completion dynamic ... dispatch instruction **issue**

instruction retirement (commit ... operands 4. _____ **map** register operand ...
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... issue width 1 in-order 4 **out-of-order** 8 **out-of-order** ... 4-issue **instruction** cache. It is able to **map** 32KB of the original program into compressed bytes. ...

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"issue instruction" "map" "out-of-"

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